WHAT IS CLAIMED IS:

1. A display drive control device comprising:

a power supply circuit which generates a plurality of voltages for displaying an image on a display device having a plurality of pixels; and

a power supply sequencer which operates based on a plurality of first registers in which a plurality of setting values for controlling said power supply circuit are set,

wherein said power supply sequencer controls said power supply circuit based on a setting value set to each register containing said plurality of first registers and outputs a signal for time control of said plurality of voltages based on predetermined time.

2. The display drive control device according to claim 1,

wherein said display device is a liquid crystal display panel comprising:

a plurality of source electrode wirings which extend along one direction and are disposed along another direction crossing said direction;

a plurality of gate electrode wirings which extend along said another direction and are disposed along said one direction;

a pixel circuit having an active element which is provided at each crossing of said source electrode wiring and said gate electrode wiring and is coupled to said source electrode wiring

and said gate electrode wiring;

a pixel electrode driven by said pixel circuit; and

a common electrode wiring coupled to a common electrode provided for said pixel electrode via liquid crystal; and

wherein said display drive control device is a liquid crystal drive controller which controls image display on said liquid crystal display panel.

3. The display drive control device according to claim 2,

wherein said liquid crystal drive controller comprises:

a source driver which supplies display data to said source electrode wiring based on a first one of said plurality of voltages supplied from said power supply circuit;

a gate driver which supplies a scan voltage to said gate electrode wiring based on a second one of said plurality of voltages supplied from said power supply circuit;

a common electrode driver which supplies a common voltage to said common electrode wiring based on a third one of said plurality of voltages supplied from said power supply circuit; and

a driver control circuit which controls said source driver, said gate driver, and said common electrode driver, and generates signals synchronized with outputs from said drivers.

4. The display drive control device according to claim 3,

wherein said power supply circuit comprises:

a reference voltage generation circuit which generates a reference voltage based on a voltage supplied from main power supply;

a booster circuit which boosts said reference voltage to a specified voltage;

a gradation voltage generation circuit which generates a display data voltage supplied to said source electrode wiring based on a first boost voltage boosted by said booster circuit;

a gate voltage generation circuit which generates a scan voltage supplied to said gate electrode wiring based on a second boost voltage boosted by said booster circuit; and

a common voltage generation circuit which generates a common voltage supplied to said common electrode wiring based on a third boost voltage boosted by said booster circuit.

5. The display drive control device according to claim 4,

wherein said plurality of first registers constituting said power supply sequencer comprise:

a second register to register a setting value for setting an operation of said booster circuit;

a third register to register a setting value for setting an operation of said gradation voltage generation circuit;

a fourth register to register a setting value for setting an operation of said power supply circuit; and

a fifth register to register a setting value for setting an operation of said common voltage generation circuit.

6. The display drive control device according to claim 1, comprising:

first setup means for determining whether or not to use said power supply sequencer; and

second setup means for starting and stopping sequence control of said power supply sequencer,

wherein said display drive control device is fabricated over one semiconductor substrate.

7. The display drive control device according to claim 6, comprising:

third setup means for setting a timing to validate setting values registered to said plurality of first registers.

8. The display drive control device according to claim 7, comprising:

a plurality of second registers to set timing for validating setting values registered to said plurality of first registers.

9. The display drive control device according to claim 8, comprising:

a plurality of third registers to set a power supply state before validation of setting values registered to said plurality of first registers; and

a fourth register to determine whether or not to provide

a plurality of registers constituting said plurality of third registers with setting values registered to said plurality of first registers.

10. The display drive control device according to claim 8,

wherein said power supply sequencer comprises:

a frame counter to count frame frequencies of said display device so as to set a timing to validate setting values registered to said plurality of first registers;

a comparator to compare setting values registered to said plurality of second registers with a count value in said frame counter; and

selection means for selecting any of setting values registered to said plurality of first registers and setting values registered to a plurality of registers constituting said plurality of third registers based on comparison outputs from said comparator.

11. The display drive control device according to claim 8, comprising:

a fifth register to register a setting value for determining whether or not to use said power supply sequencer;

a sixth register to register a setting value for determining whether or not to perform an operation of said power supply sequencer; and

a seventh register to register a setting value for

determining a termination time for an operation of said power supply sequencer.

12. The display drive control device according to claim 8,

wherein said display drive control device includes a driver control circuit,

wherein said driver control circuit includes said power supply sequencer, and

wherein said power supply control circuit controls said display drive control device and, based on a setting value registered to each register, generates a signal to generate said plurality of voltages in a time-sharing manner by controlling said power supply sequencer and said power supply circuit.

13. The display drive control device according to claim 5,

wherein said second register is capable of setting a booster magnification, a booster clock division ratio, and an operating/nonoperating state of said booster circuit,

wherein said third register is capable of setting an on/off-state of said gradation voltage generation circuit,

wherein said fourth register is capable of setting an on/off-state of said power supply circuit and the amount of current flowing through said power supply circuit, and

wherein said fifth register is capable of setting an

on/off-state of said common voltage generation circuit.

14. The display drive control device according to claim 13,

wherein said liquid crystal drive controller includes a driver control circuit,

wherein said driver control circuit includes said power supply sequencer,

wherein said driver control circuit controls said liquid crystal drive controller and, based on a setting value registered to each register, generates a signal to generate said plurality of voltages in a time-sharing manner by controlling said power supply sequencer and said power supply circuit, and

wherein said driver control circuit comprises:

an interface circuit to incorporate data from an outside;

graphics RAM to store display data;

an instruction register provided between said interface circuit and said power supply sequencer; and

a timing generation circuit to generate a timing signal as a reference of operations of said display drive control device.

15. A drive method of a display drive control device, said display drive control device comprising:

a power supply circuit to generate a plurality of voltages for displaying an image on a display device comprising a plurality of pixels in a matrix;

a plurality of first registers to register a plurality of setting values for controlling said power supply circuit;

a power supply sequencer to provide time control for said power supply circuit based on setting values registered to said plurality of first registers;

an interface circuit to interchange data with an outside; and

an instruction register provided between said interface circuit and said power supply sequencer,

said display drive control device being supplied with power from a main power supply,

wherein said drive method of said display drive control device is constituted such that after said main power supply stops supplying power, and then restarts supplying power, setting values for turning off said display device are registered to registers in said power supply sequencer and to said instruction register.

16. The drive method of the display drive control device according to claim 15,

wherein said display device is a liquid crystal display device, comprising:

many source electrode wirings which extend along one direction and are disposed along another direction crossing said direction;

many gate electrode wirings which extend along said

another direction and are disposed along said one direction;

a pixel circuit having an active element which is provided at each crossing of said source electrode wiring and said gate electrode wiring and is coupled to said source electrode wiring and said gate electrode wiring;

a pixel electrode driven by said pixel circuit; and

a common electrode wiring coupled to a common electrode provided for said pixel electrode via liquid crystal;

wherein said display device comprises:

a source driver which supplies display data to said source electrode wiring based on a first one of said plurality of voltages supplied from said power supply circuit;

a gate driver which supplies a scan voltage to said gate electrode wiring based on a second one of said plurality of voltages supplied from said power supply circuit;

a common electrode driver which supplies a common voltage to said common electrode wiring based on a third one of said plurality of voltages supplied from said power supply circuit; and

a driver control circuit which controls operations of said drivers,

wherein said driver control circuit controls said source driver, said gate driver, and said common electrode driver, and generates signals synchronized with outputs from said drivers.

17. The drive method of the display drive control device according to claim 16,

wherein said power supply circuit comprises:

a reference voltage generation circuit which generates a reference voltage based on a voltage supplied from said main power supply;

a booster circuit which boosts said reference voltage to a specified voltage;

a gradation voltage generation circuit which generates a display data voltage supplied to said source electrode wiring based on a first boost voltage boosted by said booster circuit;

a gate voltage generation circuit which generates a scan voltage supplied to said gate electrode wiring based on a second boost voltage boosted by said booster circuit; and

a common voltage generation circuit which generates a common voltage supplied to said common electrode wiring based on a third boost voltage boosted by said booster circuit,

wherein said power supply sequencer comprises first, second, third, and fourth registers,

wherein said first register registers a setting value for starting said booster circuit,

wherein said second register registers a setting value for starting said gradation voltage generation circuit,

wherein said third register registers a setting value for starting said power supply circuit, and

wherein said fourth register registers a setting value for starting said common voltage generation circuit.

18. The drive method of the display drive control device according to claim 17,

wherein said power supply sequencer comprises first and second setup means,

wherein said first setup means determines whether or not to use said power supply sequencer, and

wherein said second setup means starts and stops sequence control of said power supply sequencer.

19. The drive method of the display drive control device according to claim 18,

wherein said power supply sequencer has third setup means, and

wherein a timing to validate setting values registered to a plurality of registers constituting said power supply sequencer is set in said third setup means.

20. The drive method of the display drive control device according to claim 19,

wherein said power supply sequencer has fifth, sixth, and seventh registers each of which comprises a plurality of registers,

wherein said fifth register registers a power supply state before validation of setting values registered to said plurality of registers,

wherein said sixth register registers a timing to validate setting values registered to a plurality of registers constituting said first through fourth registers, and

wherein said seventh register specifies whether or not to register said previous power supply state to a plurality of registers constituting said fifth register.

21. The drive method of the display drive control device according to claim 20,

wherein said power supply sequencer has a frame counter, comparison means, and selection means,

wherein said frame counter counts a frame frequency on said liquid crystal display panel so as to set a timing to validate setting values registered to a plurality of registers constituting said first through fourth registers,

wherein said comparator compares setting values registered to a plurality of registers constituting said sixth register with a count value in said frame counter, and

wherein said selection means selects any of setting values registered to a plurality of registers constituting said first through fourth registers and setting values registered to a plurality of registers constituting said fifth based on comparison outputs from said comparator.

22. The drive method of the display drive control device according to claim 17, comprising the steps of:

setting a booster magnification, a booster clock division

ratio, and an operating/nonoperating state of said booster circuit to said first register;

setting an on/off-state of said gradation voltage generation circuit to said second register;

setting an on/off-state of said power supply circuit and the amount of current flowing through said power supply circuit to said third register; and

setting an on/off-state of said common voltage generation circuit to said fourth register.

23. An electronic device comprising a display drive control device and a central processing unit,

wherein said display drive control device comprises:

a display panel comprising a plurality of pixels disposed in a matrix;

a power supply circuit to generate a plurality of voltages for displaying an image on said display panel;

a plurality of first registers to register a plurality of setting values for controlling said power supply circuit;

a power supply sequencer to provide time control for said power supply circuit based on setting values registered to said plurality of first registers;

an interface circuit to interchange data with an outside; and

an instruction register provided between said central processing unit interface circuit and said power supply

sequencer,

wherein said central processing unit controls said display drive control device.

24. The electronic device according to claim 23,

wherein said electronic device is a cellular phone, and

wherein said cellular phone comprises:

an audio interface to allow input and output of audio data to and from a microphone and a speaker;

a high frequency interface to allow input and output of signals to and from an antenna;

nonvolatile memory to store a control program and control data for said cellular phone; and

volatile memory to exchange data with said central processing unit and store and output said data.

25. The electronic device according to claim 24,

wherein said cellular phone uses said power supply sequencer when said cellular phone changes from a stand-by state to an operating state, and when said cellular phone changes from a power-off state to a power-on state.

26. A semiconductor integrated circuit comprising:

a plurality of first registers which register a plurality of setting values for controlling a power supply circuit to generate a plurality of voltages in order to display an image on a display device comprising a plurality of pixels disposed in a matrix; and

a power supply sequencer which operates based on said plurality of first registers,

wherein said power supply sequencer outputs a signal to generate said plurality of voltages at a specified time interval in a time-sharing manner and controls said power supply circuit based on setting values registered to registers including said plurality of first registers.

27. The semiconductor integrated circuit according to claim 26, comprising:

first setup means for setting a timing to validate setting values registered to said plurality of first registers.

28. The semiconductor integrated circuit according to claim 26, comprising:

second setup means for determining whether or not to use said power supply sequencer; and

third setup means for starting and stopping sequence control of said power supply sequencer.

29. The semiconductor integrated circuit according to claim 27, comprising:

a plurality of second registers to set a timing to validate setting values registered to said plurality of first registers,

wherein said plurality of second registers determine said specified time interval.

30. The semiconductor integrated circuit according to claim 29, comprising:

a plurality of third registers to set a power supply state before validation of setting values registered to said plurality of first registers; and

a fourth register to determine whether or not to provide said plurality of third registers with setting values registered to said plurality of first registers.

31. The semiconductor integrated circuit according to claim 29,

wherein said power supply sequencer comprises:

a frame counter to count frame frequencies of said display device so as to set a timing to validate setting values registered to said plurality of first registers;

a comparator to compare setting values registered to said plurality of second registers with a count value in said frame counter; and

selection means for selecting any of setting values registered to said plurality of first registers and setting values registered to said plurality of third registers based on comparison outputs from said comparator.

32. The semiconductor integrated circuit according to claim 28, comprising:

a fifth register to register a setting value for determining whether or not to use said power supply sequencer;

a sixth register to register a setting value for determining whether or not to perform an operation of said power

supply sequencer; and

a seventh register to register a setting value for determining a termination time for an operation of said power supply sequencer.

33. The semiconductor integrated circuit according to claim 29,

wherein said semiconductor integrated circuit includes a driver control circuit,

wherein said driver control circuit includes said power supply sequencer, and

wherein said power supply control circuit controls said semiconductor integrated circuit and, based on a setting value registered to each register, generates a signal to generate said plurality of voltages in a time-sharing manner by controlling said power supply sequencer and said power supply circuit.